ENGINEERING IN ADVANCED RESEARCH SCIENCE AND TECHNOLOGY

ISSN 2278-2566
Vol.01, Issue.03
June -2019
Pages: -169-179

ENERGY EFFICIENT FIN-FET BASED FULL ADDER EMPLOYING MULTIPLIER

1. M.NANDINI MEDAPATI, 2. PULAKHANDAM VANI
1. Assistant Professor, Dept. of ECE, Kakinada Institute of Engineering & Technology WOMEN"S, Korangi, A.P
2. M. Tech student, Dept. of ECE, Kakinada Institute of Engineering & Technology WOMEN"S, Korangi, A.P

ABSTRACT: In this paper, low PDP multiplier is proposed based on Full adder circuit. The full adder is designed using modified XOR/XNOR circuit. The proposed multiplier is designed using both conventional FETs and FinFETs. The designs are carried out using HSPICE tool with PTM models. The proposed multiplier using FinFETs achieves low Power Delay Product, delay and power dissipation compared to conventional MOS implementation.

Index Terms: DGFinFET, CMOS, SCE, PDP, Hybrid Full Adder (FA), Power Dissipation, Delay.

I. INTRODUCTION

Every day the demand of digital circuits, e.g., cell phones, digital signal processors and communication devices increases. The power dissipation [1] and area consumption restricts the integration of large scale circuits. The life of battery operated devices depends on the power dissipation. The demand of high speed devices with low area, power dissipation drives the researchers to focus on optimization of digital circuits. The performance of many digital electronic systems depends on the performance of arithmetic circuits, such as adders, multipliers, and dividers. The add operation however plays a major role in arithmetic circuits, many efforts has been made for efficient design of adder circuits. More attention has been kept on Full adder (FA) as the fundamental block [2] – [4]. Hence the reduction of power consumption on the full adder cell is the major criteria. This can be achieved by optimization of basic gates that involves in the designing of full adder. Two variants of Full adder circuits based on the output voltage level are proposed as full-swing and nonfull-swing full adders. Full swing full adder families are Standard CMOS, [5], complementary pass-transistor logic (CPL) [6], [7], transmission gate (TG) [8] – [10], transmission function [11], 14T (14 transistors) [12], 16T [13], [14], and hybrid pass logic with static CMOS output drive full adder (HPSC) [15] – [19] FAs. 10T [3], 9T [20], and 8T [21] are of Nonfull-swing full adder families.

II. OBJECTIVE OF THE PAPER

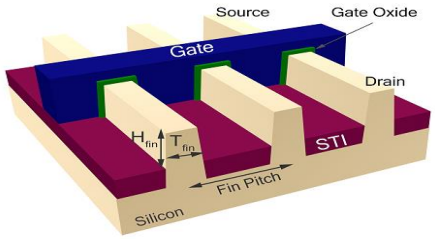
The objective of this paper is to propose a novel XOR/XNOR circuit. The hybrid full adder is implemented based on the proposed XOR/XNOR circuit. A multiplier is then designed based on the Hybrid full adder circuit. XOR/XNOR circuit, Hybrid Full Adder circuits and multiplier designs are implemented using both conventional FETs and FinFET devices. The designs are carried out using 32nm technology models. Predictive Technology Model (PTM) is used to simulate the designs using HSPICE. Performance metrics like delay, average power dissipation, and PDP are measured and comparisons are carried out between CMOS designs as well as FinFET based designs.

The rest of the paper is organized as follows, In section III, discussion are carried about FinFET technology, A clear review about the existing and proposed XOR/XNOR circuits is presented in section IV; In section V new XOR-XOR gates are presented followed by proposed full adder and multiplier, Section VI represents simulation results and their comparisons. Section VII concludes the paper.

III. FINFET TECHNOLOGY

The performance of conventional MOS devices decays with scaling due to short channel effects. FinFET's are the replacement of MOSFETs because of its low power dissipation, high performance at low operating voltages. This increases the efficiency of the FinFET designs.

FinFET devices are made in a tall and narrow silicon island called "finger", "leg" or "fin". The gate of FinFET device is wrapped around all sides of the fin. This works as the channel of the transistor. Following figure shows the cross section of FinFET device.



3D cross section view of FinFET

FinFET's are evolved from the concept of Multi Gate MOSFETs. FinFET consists of source, drain and gate terminals. In Dual Gate (DG) FETs, there are two gates, Front Gate and Back Gate. The minimum feature size in Multi Gate

Copyright @ 2019 **ijearst. All rights reserved.**

FETs is the Fin width not the gate length. For DG FinFET, the effective channel width is given by

$$W_{eff} = n\,(Fin_{thickness} + 2\,Fin_{height})$$

Where 'n' is no of Fins.

Fin height and effective Fin width decides the current in the FinFET. The short channel effects are minimized by the gate electrode control in all directions.

IV. REVIEW ABOUT XOR/XNOR CIRCUITS

Hybrid FAs consists of 2-input XOR/XNOR gate and 2-to-1 multiplexer [2]. The major power consumption module is XOR/XNOR gate in the FA cell. Therefore, the optimum designing of XOR/XNOR module leads to design of efficient Hybrid full adder circuits. Many circuits have been proposed to implement XOR/XNOR gate [10], [11], [15], [23], which a few examples of the most efficient ones are shown in Fig. 1 (a) to 1 (f).

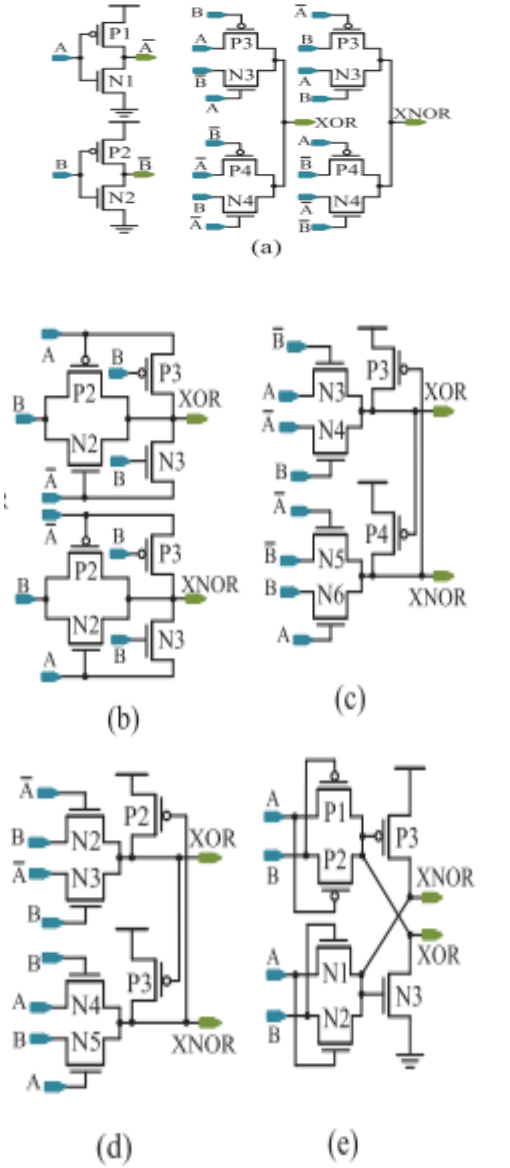


Fig 1: (a) and (b) Full-swing XOR/XNOR and (c)-(g) XOR–XNOR circuits. (a) [15]. (b) [10]. (c) [15]. (d) [2]. (e) [6], [12]. (f) [17]. (g) [22].

Fig. 1(a) shows double pass-transistor logic (DPL) style based full-swing XOR/XNOR gate circuit [15]. This structure consists of eight transistors. The two high power consuming NOT gates present in the critical path is the main problem. These NOT gates must drive the other gate inputs. In order to reduce the power consumption, the sizes of NOT gates must be increased which may cause increase in the critical path delay.

Fig.1 (b) shows six transistor based full-swing XOR/XNOR gate [10]. The delay and power consumption of PTL based XOR/XNOR logic are better than the circuit in Fig. 1(a). Fig. 1(c) shows an example of CPL logic style based XOR–XNOR circuit [15] which uses ten transistors. The feedback on the outputs is the problem in this XOR–XNOR circuit. This increases the delay and short-circuits power.

To reduce the power dissipation, Goel et al. [2] as in Fig. 1(d) removed NOT gates from the XOR–XNOR circuit of Fig. 1(c). In [6] and [12], full-swing XOR–XNOR gate with complementary feedback transistors (N3 and P3) to restore weak logic output nodes in Fig. 1(e) with only six transistors. Chang et al. [17] have proposed a new structure for the simultaneous cells of XOR–XNOR gate [shown in Fig. 1(f)] by improving the six-transistor XOR–XNOR circuit of Fig. 1(e). The main problem of this circuit is that it imposes extra parasitic capacitance to the XOR and XNOR output nodes. Thus, the delay and power consumption significantly increase. Fig. 1(g) [22] shows another circuit by improving the structure of Fig. 1(e). In this improved structure, a NOT gate is used to improve the circuit speed. To achieve all advantages by reducing the disadvantages of all the XOR/XNOR circuits, and by combining two circuits XOR and XNOR Fig. 1(a) and (b) will result in designing a new XOR-XNOR circuit. Based on the outputs and consistency of these circuits XOR-XNOR gates with highly effective output capabilities are modeled.

Copyright @ 2019 **ijearst. All rights reserved.**

TABLE I
SIMULATION RESULTS OF BOTH CMOS AND FINFET BASED EXPLORED XOR/XNOR DESIGNS @ 32-nm TECHNOLOGY WITH 0.9VPOWER (POWER IN e-6, CURRENTS AND PDP IN e-15)

SIMULATION RESULTS OF BASIC CMOS XOR/XNOR GATES							
DESIGN		DELAY (ns)	AVG POWER (uW)	PDP (fJ)	LEAKAGE CURRENT(fA)	TOT.ENERGY (fJ)	P.TOT (uW)
IA	XOR	10.1	1.921	19.96	61.07	54.6	1.364
	XNOR	10.4	2	20.03	60.67	54.91	1.37
IB	XOR	1.01	1.465	1.481	22.23	20.01	0.503
	XNOR	4.9	1.46	7.154	22.23	20.01	0.503
OVERALL IB STATUS		**5.21**	**2.81**	**14.58**	**22.23**	**20.01**	**0.503**
IC		10.28	1.639	16.75	68.31	61.54	1.53
ID		10.25	1.632	16.72	69.2	62.36	1.55
IE		10.39	1.618	16.81	36.35	32.72	0.18
IF		10.2	1.57	16.01	45.01	40.51	1.01
IG		10.49	1.521	15.73	45.32	40.78	1.01

(a)

SIMULATION RESULTS OF FINFET BASED BASIC XOR/XNOR DESIGNS						
DESIGN	DELAY (ns)	AVG POWER (uW)	PDP (fJ)	LEAKAGE CURRENT(fA)	TOT.ENERGY (fJ)	P.TOT (uW)
IA	10.02	0.149	1.42	5.24	4.71	0.71
IB	**5.001**	**0.14**	**0.7**	**3.76**	**3.38**	**0.08**
IC	10.05	0.16	1.6	7.44	6.7	0.16
ID	10.005	0.15	1.5	7.52	6.77	0.69
IE	10.003	0.7	1.7	5.67	5.11	0.127
IF	10.003	0.2	2	6.25	5.62	0.14
IG	10.002	0.18	1.2	6.39	5.75	0.143

(b)

Various Parameters in Existing circuits (a) CMOS (b) FinFET when implemented at 32nm

V. PROPOSED XOR/XNOR CIRCUIT

The proposed XOR/XNOR gate in Fig. 2 consists of 12 transistors. This is derived by combining the XOR/XNOR modules shown in Fig. 1(a) and (b). The proposed structure produces full swing output voltage for all input combinations. The structure does not have any NOT gates in the critical path so that the delay will be reduced and driving capabilities will be improved. This circuit is robustness against voltage scaling and transistor sizing model.

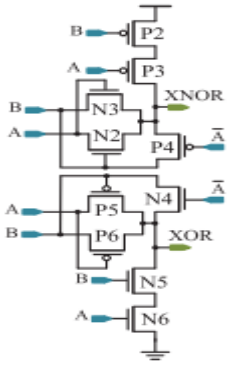


Fig 2: Proposed full-swing XOR/XNOR gate.

PROPOSED FULL ADDER AND MULTIPLIER CIRCUIT

We have proposed a Hybrid full adder circuit based on the new XOR/XNOR logic. The proposed full adder circuit is shown in Fig. 3. It consists of 22 Transistors. The Full adder (FA) is designed using the proposed XOR/XNOR module and multiplexer module. This adder dissipates less power and achieves low delay due to less capacitance of XOR/XNOR module. The performance of the designed adder is verified in both CMOS and FinFET technologies.

We have proposed simple a 4-bit multiplier circuit shown in Fig.4 which carries out 4-bit by 4-bit. The proposed multiplier is designed using the proposed hybrid full adder circuit. The multiplier is highly optimized in terms of delay and power consumption as the base full adder used for its construction is fully efficient. Simulations are carried out for both CMOS and FinFET codes.

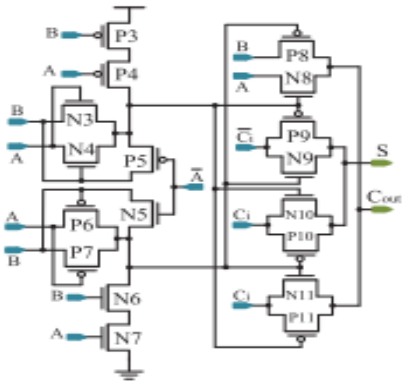
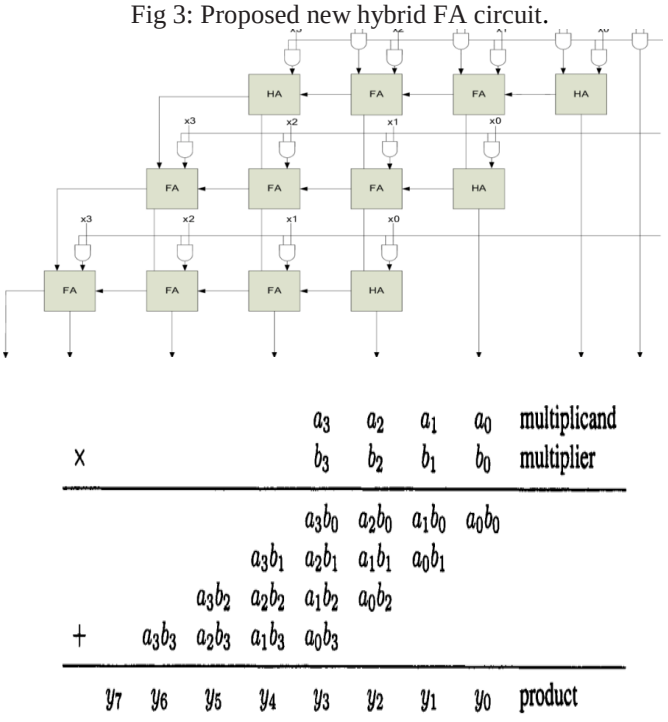


Fig 3: Proposed new hybrid FA circuit.

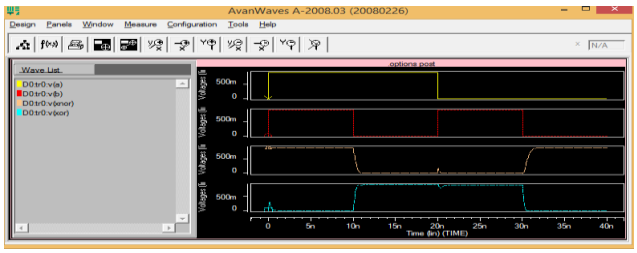


$$
\begin{array}{lccccccccc}
 & & & & a_3 & a_2 & a_1 & a_0 & \text{multiplicand} \\
\times & & & & b_3 & b_2 & b_1 & b_0 & \text{multiplier} \\
\hline
 & & & & a_3b_0 & a_2b_0 & a_1b_0 & a_0b_0 & \\
 & & & a_3b_1 & a_2b_1 & a_1b_1 & a_0b_1 & & \\
 & & a_3b_2 & a_2b_2 & a_1b_2 & a_0b_2 & & & \\
+ & a_3b_3 & a_2b_3 & a_1b_3 & a_0b_3 & & & & \\
\hline
y_7 & y_6 & y_5 & y_4 & y_3 & y_2 & y_1 & y_0 & \text{product}
\end{array}
$$

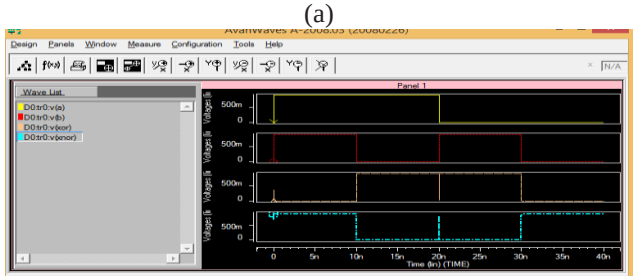
Fig 4: Block diagram of 4x4 Multiplier using the proposed full adder and its operation

The time domain results of the CMOS and FinFET designs at the scaled technology size was as shown below: The glitches formed in the CMOS circuits which effects the performance of the designs are eliminated in the Avanwaves of FinFET designs. So it can be clear that the performance will be more effective in FinFET circuits.

Copyright @ 2019 **ijearst. All rights reserved.**



(a)



(b)

Fig 5: Avanwaves of (a) CMOS XOR/XNOR gates (b) FinFET XOR/XNOR gates

VI. SIMULATION RESULTS

New XOR/XNOR, Hybrid Full Adder and multiplier circuits are implemented using 32nm CMOS and FinFET predictive technology model under [24], [25]. FinFETs are advantageous than conventional MOSFETs due to their low leakage currents and subthreshold currents [26]. The parameters used to simulate the circuits are given in the following tables:

TABLE II: 32nm CMOS TECHNOLOGY MODEL PARAMETERS

Parameter	Value
Technology node	32nm
Supply voltage	0.9
Threshold voltage of PMOS	-0.45
Threshold voltage of NMOS	0.5
Width and length of PMOS	W=128n L=32n
Width and length of NMOS	W=64n L=32n

TABLE III: FINFET 32nm TECHNOLOGY MODEL PARAMETERS

Parameter	Value
Technology	32nm
Supply voltage	0.9
Fin length	32nm
No of fins	1
Threshold voltage NMOS	0.29
Threshold voltage PMOS	-0.25
Width and length of PMOS	W=128n,L=32n
Width and length of NMOS	W=64n L=32n

TABLE IV
RESULT COMPARISION TABLE
@ 32-nm TECHNOLOGY WITH 0.9VPOWER
(POWER IN e-6, CURRENTS AND PDP IN e-15)

	POWER DISSIPATION		LEAKAGE CURRENTS		PDP	
DESIGN	CMOS	FINFETS	CMOS	FINFETS	CMOS	FINFETS
IA	1.926	0.149	61.07	5.24	20.03	1.428
IB	**2.819**	**0.14**	**22.23**	**3.76**	**14.58**	**0.701**
IC	1.639	0.16	68.31	7.44	16.75	1.6
ID	1.632	0.15	69.2	7.52	16.72	1.51
IE	1.618	0.17	36.35	5.67	16.81	1.7
IF	1.57	0.2	45.01	6.25	16.01	2
IG	1.521	0.18	45.32	6.39	15.73	1.2

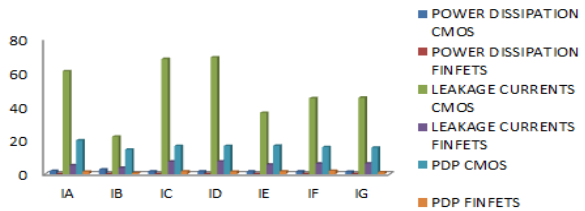
(a)

COMPARISION OF VARIOUS PARAMETERS		
PARAMETER & DESIGN	CMOS	FINFET
DELAY(ns)	10.21	10.002
POWER DISSIPATION(uW)	1.19	0.07
PDP(fJ)	12.13	0.7
LEAKAGE CURRENT(fA)	21.1	2.6
TOT.ENERGY(fJ)	19.5	2.31
P.TOT(uW)	0.47	0.058

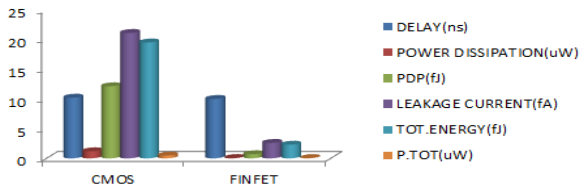
(b)

Variations of different parameters in (a) Existing circuits. (b) Proposed XOR-XNOR circuit

Proposed XOR/XNOR circuit is implemented using both conventional FETs and FinFETs at 32nm size. The achieved results are compared with the XOR/XNOR circuits discussed in section III in terms of delay, power dissipation and PDP. The proposed XOR/XNOR achieves low PDP than other circuits.



(a)



(b)

Fig 6: Different parameters models in (a) Existing XOR/XOR designs (b) Proposed XOR/XOR designs implementations

Copyright @ 2019 **ijearst. All rights reserved.**

COMPARISION OF VARIOUS PARAMETERS		
PARAMETER & DESIGN	CMOS	FINFET
DELAY(ns)	2.14	2.134
POWER DISSIPATION(uW)	4.37	0.181
PDP(fJ)	9.032	0.421
LEAKAGE CURRENT(fA)	11.4	1.726
TOT.ENERGY(fJ)	10.03	1.654
P.TOT(uW)	2.5	0.163

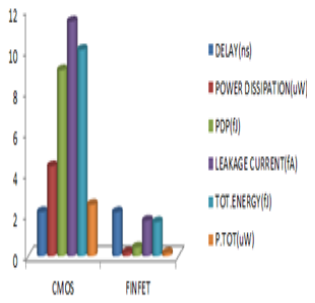


Fig 7: Different parameters in Full Adder designs CMOS Vs FinFET's

The proposed full adder and multiplier are implemented using both the conventional and FinFET devices. The results are compared in terms of PDP, power dissipation and delay. FinFET based designs reduce power dissipation, PDP compared to conventional FET based designs. This is due to the dual gate structure of FinFET transistors which reduces the leakage currents at the junction terminals. Due to this the stability of the design increases until minimum scalability ranges.

TABLE V
SIMULATION RESULTS OF CMOS AND FinFET MULTIPLIER DESIGN USING PROPOSED FULL ADDER @ 32-nm TECHNOLOGY WITH 0.9VPOWER (POWER IN e-6, CURRENTS AND PDP IN e-15)

DIFFERENT PARAMETERS IN MULTIPLIER DESIGN USING FULL ADDER		
DESIGN	CMOS	FINFET
DELAY	0.91	0.481
LEAKAGE CURRENTS	2.9	0.404
POWER DISSIPATION	81.9	14.53
PDP	74.52	6.989

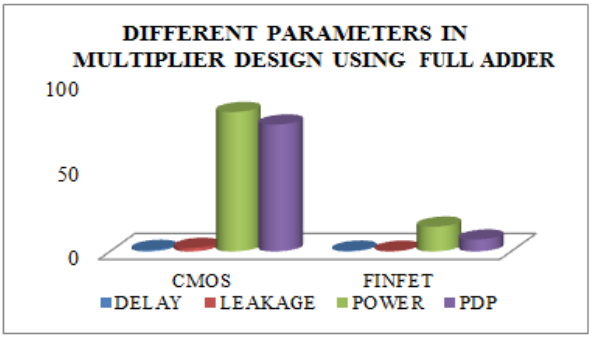


Fig 8: Different parameters in Multiplier designs CMOS Vs FinFET's

VII. CONCLUSION

It is observed that FinFETS are capable to overcome the limitations of CMOS devices most effectively. FinFET due to its dual gate structure have significantly faster switching times, excellent control over SCE and higher current density than the mainstream CMOS technology. The result comparisons at 32nm technology potentially offer a 50-60% performance increase and a 50% power reduction compared to earlier designs. The results obtained from the simulation of these designs help to prove that FinFETs can be used to reduce power without compromising the performance.

REFERENCES

[1] N.S.Kim et al., "Leakage current: Moore's law meets static power," Computer, vol. 36, no. 12, pp. 68–75, Dec. 2003.

[2] S.Goel, A.Kumar, and M.Bayoumi, "Design of robust, and the totally highly energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 12, pp. 1309–1321, Dec. 2006.

[3] H.T.Bui, Y.Wang, and Y.Jiang, "Design and analysis and verification on the paper of low-power 10-transistor full adders using novel XOR-XNOR gates," by the exploration of IEEE Trans. Circuits Syst. II, Analog Digit. Signal Processing Jan. 2002.

[4] S.Timarchi and K.Navi, "Arithmetic circuits of redundant UT-RNS," IEEE Trans. Instrum. Meas., vol. 58, no. 9, pp. 2959–2968, Sep. 2009.

[5] J.M.Rabaey, A.P.Chandrakasan, and B.Nikolic, Digital Integrated Circuits, vol. 2. Englewood Cliffs, NJ, USA: Prentice-Hall, 2002.

[6] D.Radhakrishnan, "Low-voltage low-power CMOS full adder," IEEE Proc.-Circuits, in 2001.

[7] K.Yano, A.Shimizu, T.Nishida, M.Saito, and K.Shimohigashi, "A 3.8-ns CMOS 16×16-b multiplier using the complementary pass-transistor logic," IEEE J.Solid-State Circuits, vol. 25, no. 2, pp. 388–395, Apr. 1990.

[8] A.M.Shams, T.K.Darwish, and M.A.Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 10, no. 1, pp. 20–29, Feb. 2002.

[9] M.Zhang and H.Wu, "A new design of the CMOS full adder designing from IEEE paper J. Solid-State Circuits, vol. 27, no. 5, pp. 840–844, May 1992.

[10] N.Weste and K.Eshraghian, Principles of CMOS VLSI Design. New York, NY, USA: Addison-Wesley, 1985.

[11] P.Bhattacharyya, B.Kundu, S.Ghosh, V.Kumar, and A.Dandapat, "Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23,no. 10, pp. 2001–2008, Oct. 2015.

[12] M.Vesterbacka, "A 14-transistor CMOS full adder with full voltage swing nodes," in Proc. IEEE Workshop Signal Process. Syst. (SiPS), Oct. 1999, pp. 713–722.

[13] M.Alioto, G.DiCataldo, and G.Palumbo, "Mixed full adder topologies for high-performance low-power arithmetic

Copyright @ 2019 **ijearst. All rights reserved.**

circuits," Micro electron. J. vol. 38, no. 1, pp. 130–139, 2007.
[14] A.M.Shams and M.A.Bayoumi, "A novel high-performance CMOS1-bit full-adder cell," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process. vol. 47, no. 5, pp. 478–481, May 2000.
[15] M.Aguirre-Hernandez and M. Linares-Aranda, "CMOS full-adders for energy-efficient arithmetic applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 4, pp. 718–721, Apr. 2011.
[16] I.Hassoune, D.Flandre, I.O'Connor, and J.D.Legat, "ULPFA: A new efficient design of a power-aware full adder," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 8, pp. 2066–2074, Aug. 2010.
[17] C.H.Chang, J.Gu, and M. Zhang, "A review of 0.18-μm full adder performances for tree structured arithmetic circuits," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 6, pp. 686–695, Jun. 2005.
[18] P.Kumar and R.K.Sharma, "Low voltage high performance hybrid full adder," Eng. Sci. Technol., Int. J., vol. 19, no. 1, pp. 559–565, 2016.
[19] M.Ghadiry, M.Nadi, and A.K.A. Ain, "DLPA: Discrepant low PDP 8-bit adder," Circuits Syst. Signal Process., vol. 32, no. 1, pp. 1–14, 2013.
[20] S.Wairya, R.K.Nagaria, and S.Tiwari, "New design methodologies for high-speed low-voltage 1 bit CMOS Full Adder circuits," Int. J.Comput. Technology.
[22] S.R.Chowdhury, A.Banerjee, A.Roy, and H.Saha, "A high speed 8 transistor full adder design using novel 3 transistor XOR gates," Int. J. Electron., Circuits Syst., vol. 2, no. 4, pp. 217–223, 2008.
[23] M.A.Valashani and S.Mirzakuchaki, "A novel fast, low-power and high-performance XOR-XNOR cell," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), vol. 1. May 2016, pp. 694–697.
[24] From site http://ptm.asu.edu/modelcard/2006/ 32nm_bulk.pm
[25] Online site http://ptm.asu.edu/modelcard/2006/ 32nm_finfet.pm
[26] Vejendla, N.Reddy, R.Balaji, N. (2017). Performance Analysis of Adder Circuits Using FINFET'S. i-manager's Journal on Circuits and Systems.

Copyright @ 2019 **ijearst. All rights reserved.**